ARN-21D Solid State **Modulator - A/A mode**

Power Requirements for the solid state air-to-air modulator shall not exceed the following under any combination of normal operating conditions:

0.5	Ampere	@	124 volts RMS, 320 to 1000 cps
0.25	Ampere	@	29 Vdc
0.16	Ampere	@	120V dc
1.5	mA	@	-100 or –180V dc

Specifically, the solid state air-to-air modulator contains the following circuits:

(1)	Interrogation PRF Generator	27 Hz or 150 Hz
(2)	Interrogation Encoder	12μs interpulse time
(3)	Transmission Pulse Shaping	Gaussian, 3μs at 50% height
(4)	A/A decoder	Reply all double pulses except at early gate
(5)	A/A System delay	62 μs total
(6)	A/A AGC	2 sec time constant for low pulse rate
(7)	A/A Over-Interrogation Countdown	max. 1250 pulses/s
(8)	Transmitter Muting	also on A/A – T/R switchover to protect mixer
(9)	First Pulse generator Dead Time	125 μs

Automatic Gain Control (A/A) - An adjustable air-to-air AGC shall be provided such that it is possible to reject the weaker of two signals when they differ by an amount between 15 and 35dB. This AGC shall be generated by properly coded interrogations and shall require no more than 2 seconds to reach 90% of the final value determined by any instantaneous change in the interrogation signal level.

Transmitter Power (A/A) - When the total transmission rate is between 22 and 30 pulse pairs per second, the peak power shall be the same as that transmitted in the normal mode when tracking a distance reply signal from a ground beacon. A maximum reduction in peak power of 3 db is permissible when the total transmission rate is 1050 pulses per second.

Transmitter Muting – Satisfactory muting of the transmitter shall be provided during channel selection in the air-to-air mode and in the T/R mode, as well as while switching from A/A to T/R or from T/R to A/A to protect the mixer diode.

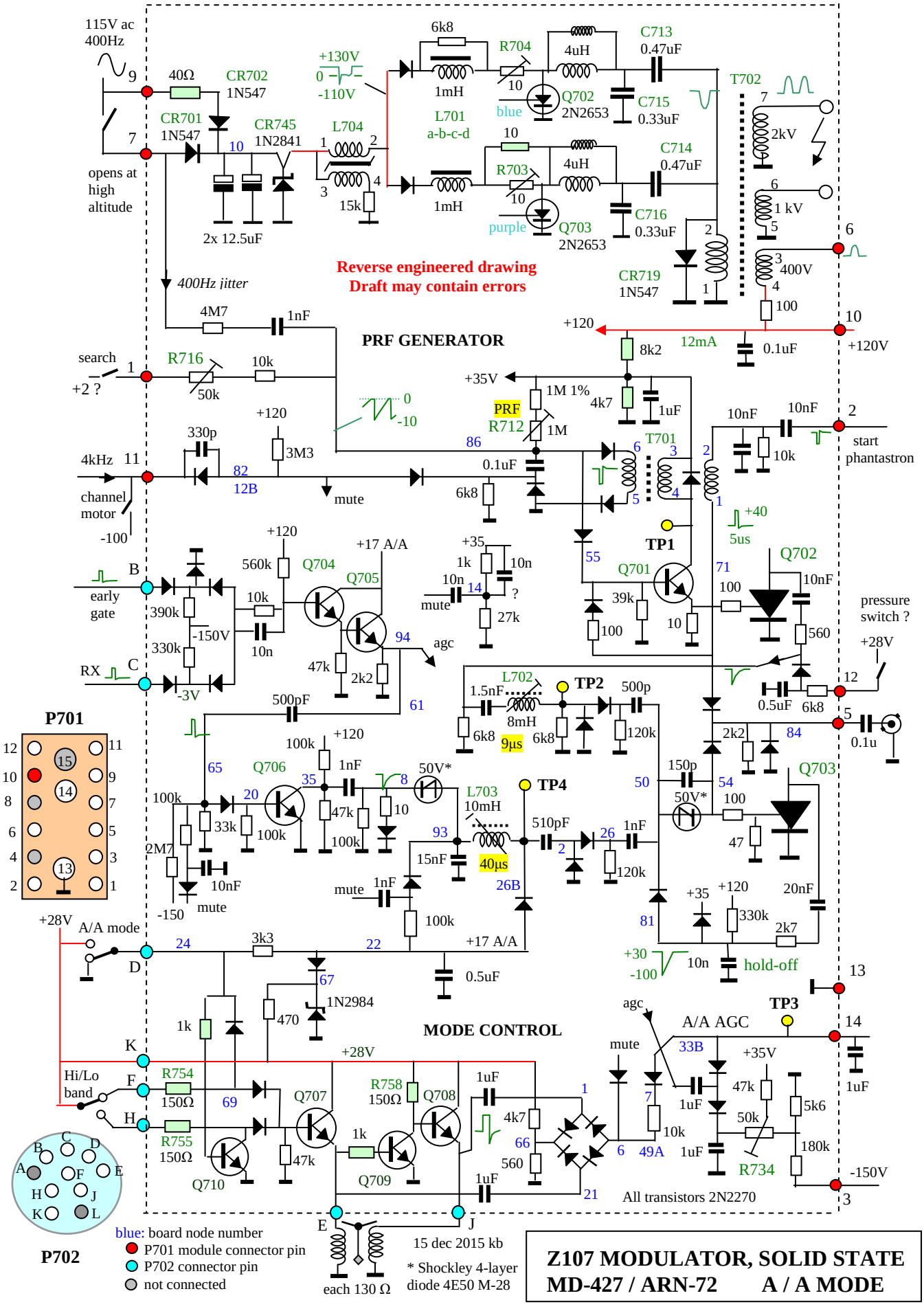
Over-interrogation – The transmitter shall not be capable of transponding at a rate in excess of 1250 pulses per second.

System Delay (A/A) - The transponder reply pulse shall occur 62 ± 1 microseconds after the receipt, at the antenna terminal, of the first pulse of a coded interrogation pair. The distance indicator of the interrogating Radio Set AN/ARN-21D shall display 0 ± 0.1 miles upon receipt of a reply pulse at its antenna terminal 62 microseconds after transmission of the first interrogation pulse.

Dead time gate – All time shared random triggers, both interrogations and reply, shall be inhibited for 125 ± 25 microseconds after the generation of either the first interrogation pulse or an air-to-air reply pulse.

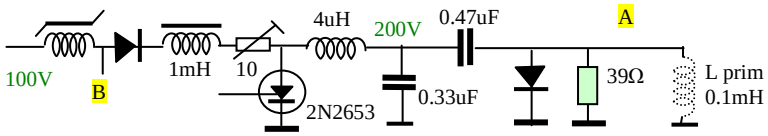
Adjustments - Screwdriver adjustments shall be provided to set the interrogation PRF, the interrogation pulse pair spacing, the air-to-air system delay time, and the air-to-air AGC.

Interrogation sync – An interrogation sync terminal shall be provided on the modulator chassis. The terminal shall be readily accessible when the receiver-transmitter dust cover is removed for maintenance or test.

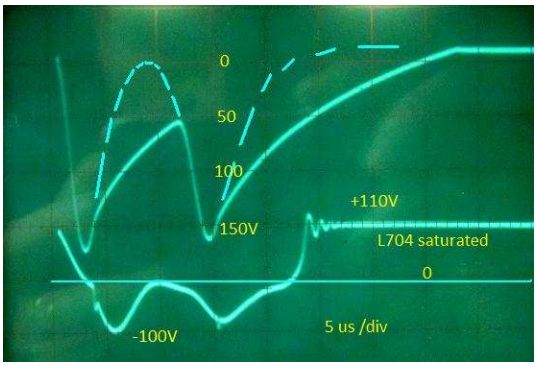

115V ac
400Hz
9
7
opens at high altitude
40Ω
CR702
1N547
CR701
1N547
CR745
1N2841
10
2x 12.5uF
+130V
0
-110V
L704
1
2
3
4
15k
6k8
1mH
L701
a-b-c-d
R704
10
blue
Q702
2N2653
4uH
C713
0.47uF
C715
0.33uF
R703
10
purple
Q703
2N2653
4uH
C714
0.47uF
C716
0.33uF
CR719
1N547
T702
7
2kV
6
1 kV
5
3
400V
4
100
6
10
+120V
12mA
0.1uF
8k2
+120
400Hz jitter
4M7
1nF
PRF GENERATOR
search
+2 ?
1
R716
50k
10k
+35V
1M 1%
4k7
1uF
PRF
R712
1M
0
-10
330p
+120
3M3
4kHz
11
82
12B
mute
86
0.1uF
6k8
T701
6
3
2
5
4
1
10nF
10nF
10k
2
start phantastron
channel motor
-100
+40
5us
TP1
55
Q701
71
Q702
100
10nF
560
pressure switch ?
+28V
B
early gate
390k
-150V
330k
RX
C
-3V
+120
560k
Q704
Q705
10k
10n
+17 A/A
+35
1k
10n
10n
14
?
mute
27k
94
agc
47k
2k2
39k
100
10
500pF
61
L702
1.5nF
8mH
TP2
500p
6k8
9µs
6k8
120k
0.5uF
6k8
12
5
0.1u
2k2
84
P701
12
10
8
6
4
2
11
9
7
5
3
1
15
14
13
65
Q706
100k
+120
1nF
35
8
50V*
20
100k
33k
100k
47k
100k
10
L703
10mH
TP4
93
510pF
26
1nF
120k
2M7
10nF
-150
mute
15nF
40µs
26B
mute
1nF
100k
+17 A/A
50
54
150p
50V*
100
47
Q703
+28V
A/A mode
D
24
3k3
22
0.5uF
67
1N2984
470
1k
MODE CONTROL
81
+35
+120
330k
20nF
2k7
+30
-100
10n
hold-off
13
agc
TP3
A/A AGC
14
mute
33B
+35V
47k
5k6
1uF
1uF
50k
180k
R734
-150V
3
All transistors 2N2270
K
Hi/Lo band
F
H
R754
150Ω
R755
150Ω
69
Q707
Q710
47k
+28V
R758
150Ω
Q708
Q709
1k
1uF
4k7
66
560
1uF
1
7
10k
6
49A
1uF
21
E
J
each 130 Ω
15 dec 2015 kb
* Shockley 4-layer diode 4E50 M-28
P702
A
B
C
D
E
F
H
J
K
L
blue: board node number
P701 module connector pin
P702 connector pin
not connected
Reverse engineered drawing
Draft may contain errors
Z107 MODULATOR, SOLID STATE
MD-427 / ARN-72 A / A MODE

Description of circuit parts

Pulse forming network

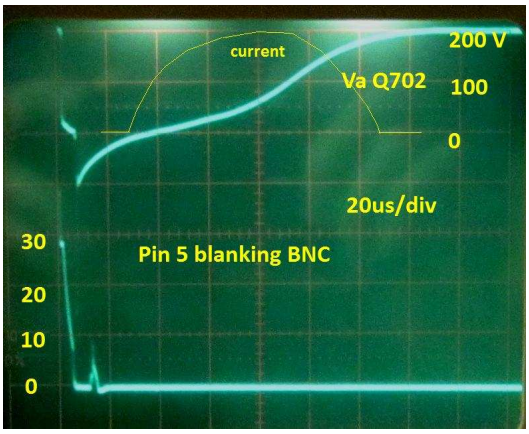


Each PFN has two capacitors (0.33uF and 0.47uF), both charged to twice the input voltage.
After the pulse there is a negative voltage across the thyristor for commutation.



The input voltage here was only 100Vdc, and the pulse output was minus 170V peak into a 39 Ω resistor that was used as dummy load instead of the HV xformer.

The upper trace shows this output voltage at point "A" in the diagram above, while the lower trace "B" shows the input voltage after the saturating choke.
The dotted line shows the simulated waveform when the main inductance of the primary is added.



The capacitors of the pulse forming network (PFN) are recharged via an 1mH choke to twice the DC voltage, resulting in a 90us half cycle charging current with a peak value of 2A.

Choke L704 isolates the thyristor discharge from the DC input circuit until 24us after the start of the first pulse, when choke L704 saturates from approx. 1H down to 0.1mH.

The stored energy in each PFN is 0.5 x 0.8uF x $200V^2$ = 16mJ, enough for a 5kW x 3us pulse.
The peak thyristor current is 75A, a negative Vak is present for 20 us to recover the thyristor.

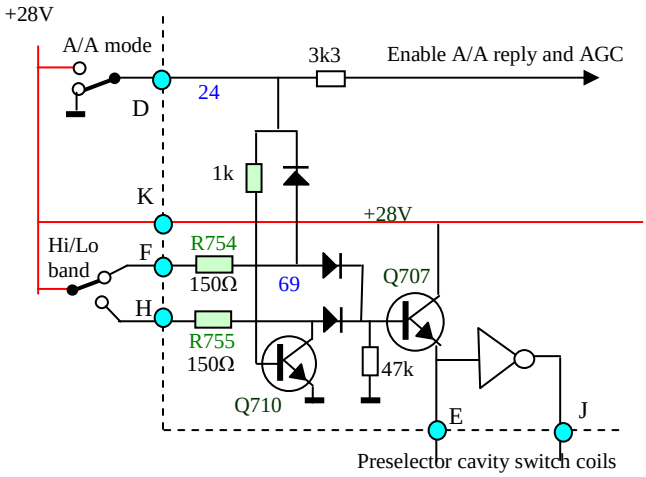
Muting

The transmitter is muted when
- pin 11 is tied to -100V when the channel selector motor runs (as in ARN21-B and -C)
- when the preselector cavity coils change state. This happens when the ch 62-63 border is passed, or when the A/A mode is switched on or off.

A/A mode switching

The change from normal mode to the Air-to-Air (A/A) mode requires the following actions:
- Bypass the twin-pulse detection in the receiver (use only the 12us delayed video);
- Enable the reply on any interrogation except the one that coincides with the early gate in the range tracking circuit ;
- Swap the control wires to the prescaler cavity ;
- Use slower Automatic Gain Control (AGC).

For these functions, an extra connector P702 is added to the modulator.



In normal mode, input F is made inoperative, and
- when the hi-lo switch pulls H high, then Q707 conducts, so E is high (and J is low)
- when the hi-lo switch pulls F high, then Q707 conducts not, so E is low (and J is high)

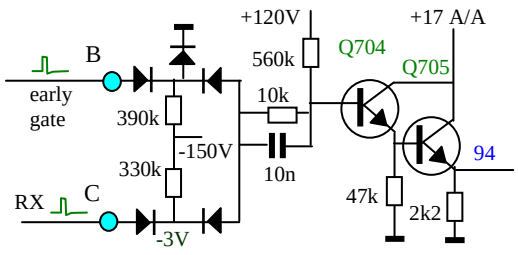
In A/A mode, input H is made inoperative, so
- when the hi-lo switch pulls H high, then Q707 conducts not, so E is low (and J is high)
- when the hi-lo switch pulls F high, then Q707 conducts, so E is high (and J is low)

When the new modulator is placed in an original ARN21B or C chassis, then connector P702 stays in its storage position, and the hi/lo switch connects directly to the normal preselector cavity switch coils.

Pulse Repetition Frequency (PRF) generator. The generator has a slowly charging capacitor and a blocking oscillator around Q701. When the capacitor voltage rises above +1V then Q701 starts to conduct, and stays on due to positive feedback until the core of T701 saturates which blocks T701. During the (5µs) pulse, the timing capacitor gets a negative shot, and the cycle repeats. The pulse triggers thyristor Q702, and starts the range circuit in the ARN21.

Second pulse delay.
The negative slope (200V in 3us) on the anode of thyristor Q701 starts a delay of 9us around L702, so the time from triggering Q702 until triggering of Q703 is 12 µs. This gives the second pulse as required in normal Tacan operation.

Received pulses.
In A/A mode, the airborne set shall respond any received dual pulse with a single pulse such that the delay from the first received pulse until the response pulse is 62 µs. Only a received pulse that coincides with the range gate shall *not* be retransmitted to prevent eternal retransmission.



The receive gate circuit has 5 diodes. The voltage between the diodes is -3V with open inputs, and only the two output diodes conduct. Base voltage of Q704 is negative and both transistors are off.
But how this works ....

A/A system delay
The group delay in the IF strip is 5us, the video input delay line adds 12us, and the detection delay of the range circuit is 3us. The delay of the modulator is 3us, so the delay circuit around L703 of 39us was added to bring the total system delay to 62us.

AGC
In A/A mode, only 20 single pulses per second may be received , instead of 2700 twin pulses in normal Tacan operation. The normal ARN21 automatic gain control would fully open the IF amplifier, as if nothing was received. A special circuit in the ARN21D modulator was added to pull the AGC line negative with a 2 sec averaging time

Hold-off
A circuit around Q703 prevents further triggers for 140us. The first pulse in normal operation is not affected. This is not needed, this thyristor is fired only 20 or 150 times per second.

Coil data

Inductors

L701 a-b	charger	1mH	0.4 Ω
L701 c-6	pulseform	4 uH	0
L702	12us delay	8mH	36 Ω
L703	45us delay	10mH	36 Ω
L704	DC choke	7 H or 100uH	0.3 Ω saturates at 100V x 30us = 3 mVs (5mA)
		turns ratio 1:1	Core reset bias : 120V/ 15kΩ = 8mA
Pre selector cavity switch coils		110 Ω and 140 Ω	

Transformers

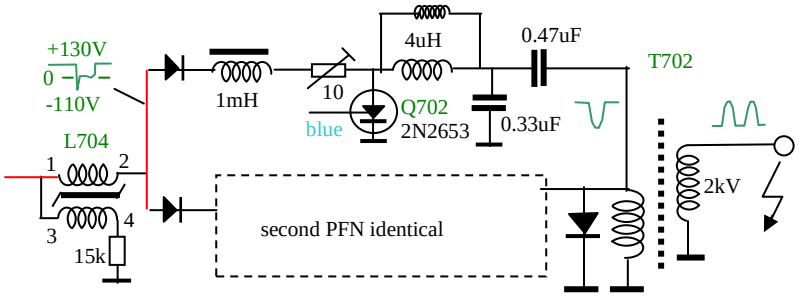
T 701	Blocking osc. 1-2	0 Ω 40V pulse (sec)
	Blocking osc. 3-4	0 Ω 25V pulse (prim)
	Blocking osc. 5-6	0 Ω 20V pulse (reset timing capacitor)
T 702	Primary 130V	0.2 Ω
	HV 2kV	14 Ω
	HV 1kV	8 Ω
	HV 400V	10 Ω

Primary impedance 1.3 mH // 266Ω // 17nF (resonant at 17 kHz)

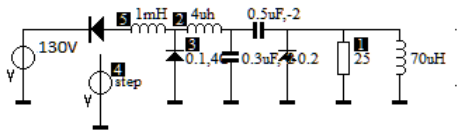
Analysis of the half-cycle LC circuits

The ARN21D modulator has many half-cycle LC- circuits:
- Power circuits forming the first or second high voltage pulse;
- The LC circuit making the 12us delay between them;
- The LC circuit that makes the system delay in the A/A mode.

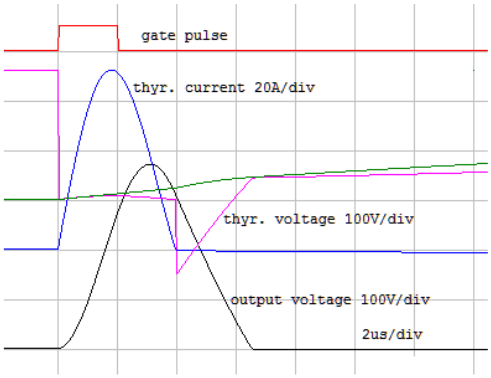
1. Pulse forming network

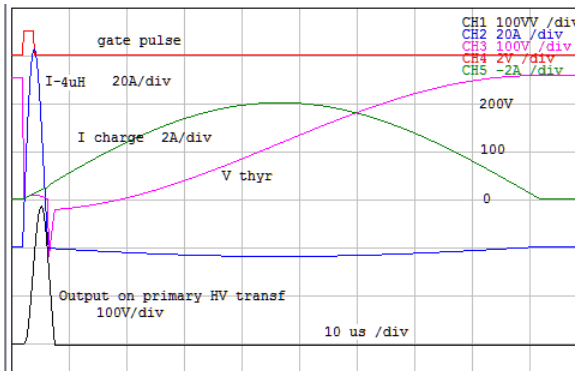


The PFN of the ARN-21D Solid State Modulator is simulated without the HV transformer, instead a 25Ω resistor is used as load, the peak output is $(300Vp)^2 / 25\Omega =$ 3.6kW peak.
The peak current in the thyristor is approx. 70A
The peak current in the recharge inductor is 4A.
To get in the simulation a positive pulse on the output, all diodes and the thyristor were inverted, and the source voltage was -130V.



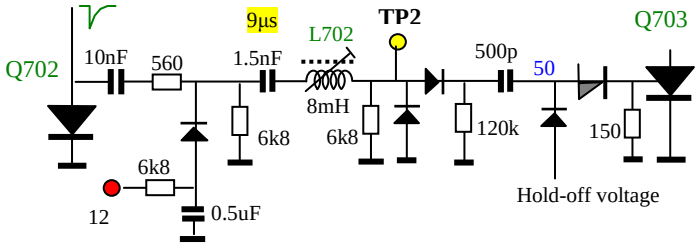
Available commutation time is 2us in the model, but 25us in reality ?!



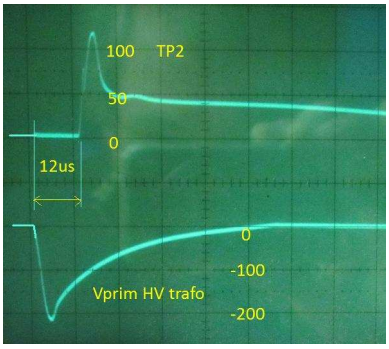


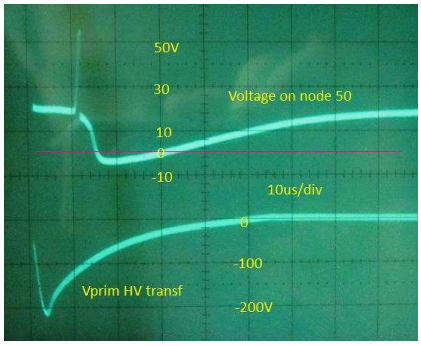
2. The 12us delay circuit

The 12us delay from first to second thyristor is needed to transmit the normal **twin** Tacan pulse

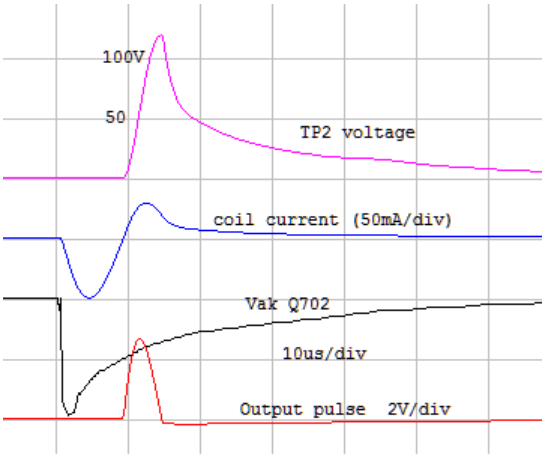


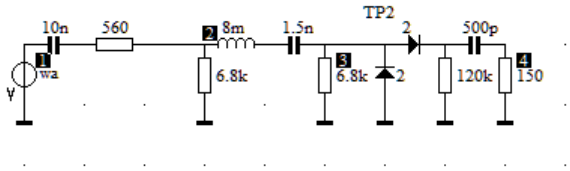
The first thyristor (Q702) is periodically triggered by the PRF generator with approx. 20 or 150 pulses per second. Each triggering causes a sharp negative slope of the anode voltage of Q702.
This negative slope causes a half cycle current surge in the 8mH and 1.5nF timing elements. After 9us, the current reverses, producing a 120V peak at testpoint TP2, and a 30V peak above the hold-off voltage at node 50. With +20V hold-off voltage, this should fire the diac and the thyristor, but it doesn't. Simulation shows that the peak at node 50 is only 3V ?!
When Q703 does fire, then the hold-off voltage drops suddenly to say -100V, and this commutates the diac and the thyristor. Otherwise the gate pulse would stay high, and the thyristor would stay on, shorting the 130V power supply...





Simulation

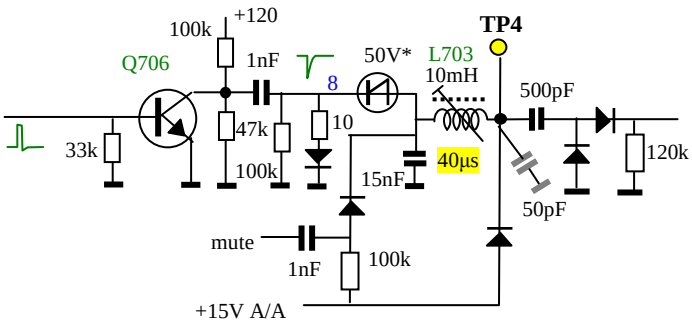


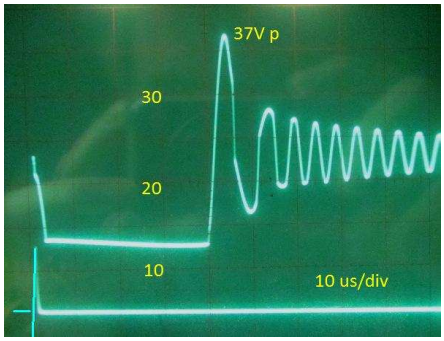


The source wave emulates the anode waveform of Q702. This is the input to the "12us" delay circuit. The large negative voltage (-100V) causes a negative half cycle current in the coil. When the current reverses, there is a moderate positive peak on the output.

Another 4-layer diode is between the output of the 40us delay circuit and the gate of Q703, biased by the hold-off voltage. Once the 4-layer diode is triggered, a dc gate current to the thyristor starts until the negative slope of its anode voltage pulls down the hold-off voltage to -100V. This ends the gate pulse, and prevents a re-trigger within 125us until the hold-off voltage is back to at least +20V.

3. The 50us delay circuit.



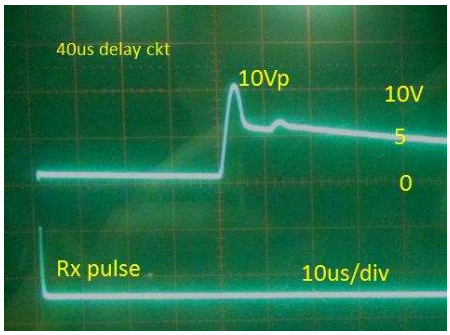


The voltage on (input) node 8 shoots to -20V until the diac breaks down, and Ccap (15nF) is discharged in 10Ω x 15nF = 0.15us. (TP4 discharges in 0.6us from 25 to 15V which is not relevant for the timing). The negative pulse on node 8 is only 50ns wide.
Then, Ccap re-charges in 40µs to +20V via the coil. The current in the coil is a half wave from right to left on the drawing. At the end of the half cycle, the current direction will reverse giving a damped oscillatory wave at 200 kHz due to the 50pF capacitance of the probe and diodes at TP4. Ccap is charged to approx. 10V *above* the +15V A/A line.

On the screenshot, TP4 is the upper trace, node 8 is the lower trace. The small negative peak is not well visible on this scale. The bottom voltage from the TP4 waveform is the "+15 A/A" bus, which is +15V at 2000 pulses/s, or +16.5V at 200 pulses/sec.

The output circuit (500pF and 2 diodes) is a peak rider, providing a waveform that can trigger the output 4-layer diode

The rest of the cycle is described in the previous 12us paragraph.



Simulation

The start pulse is simulated by a pre-charged 1nF input capacitor.