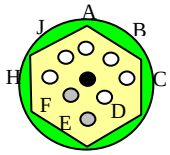
# ARC-34 Testpoints

Each module of the **AN/ARC-34** has a special 9-pole test connector to check the B+ voltages, filament voltage, and oscillator negative grid voltages.

These are measured with the URM-76A voltmeter for a quick go/no-go test on each of the 9 modules in the ARC-34. Each test connector is color coded.

The voltmeter has an 8-position switch to measure the voltage on each pin of the test connector versus the centre pin K which is grounded in each testconnector.




I measured the following voltages on a healthy set with 27Vdc input.

| Module | | A | B | C | D | E | F | H | J |
|---|---|---|---|---|---|---|---|---|---|
| Modulator | 1 | + 330 | + 307 modulated | + 330 300 Tx | +27 | | | | |
| IF Amplifier | 2 | + 117 guard | + 117 | + 117 100 Rx | +27 | -0.53 LO-2 | | | |
| Crystal Reference | 3 | + 330 | + 117 | + 129 (+130 stab) | +27 | -1.2 osc 4 | -1.13 osc.3 | -1.0 osc.2 | -2.36 osc 1 |
| Master oscillator | 4 | | + 117 | + 129 (+130 stab) | | -0.71 Sidestep | | -0.84 doubler 2 | -0.67 doubler 1 |
| Driver | 5 | + 268 Input stab | + 80 +300Tx/4 | + 117 100 Tx | +27 | | | -16.5 Driver2 | -0.41 Driver1 |
| Main Receiver | 6 | | | +117 100 Rx | +27 | | | -0.17 mixer | -0.40 tripler |
| RF Power Amp | 7 | + 308 | + 307 modulated | + 5.8 | +27 | -11.5 PA1 | -12.9 PA2 | -9.0 driver | -24.7 tripler |
| Guard Rx | 8 | | | + 117 guard | +27 | -0.16 mixer | -0.28 butler | | |
| Selector | 9 | + 330 | Gearbox See plot | + 129 (+130 stab) | +27 | | | | |

The grey positions are not connected in that module.
The blue positions shall be checked in Transmit mode ( key down)
The guard positions shall be checked with the mode switch on the control panel in the position “Both”

Modulator testpoints B and C have a 2M4 series resistor, so measure 250V on a voltmeter with 10 MΩ input impedance.
Selector testpoint B has also 2M4 series resistor, add 20% when measuring with a x10 probe
Many testpoints in the driver or RF Power Amp have 1M series resistor. Add 10%.
The readings for the oscillators in the crystal reference module are quite independent of the frequency selected.

## Tuning system

The most interesting part of the AN/ARC-34 is the tuning system, that was very advanced in 1952. It uses the sum of a minimal number of crystals in four oscillators to give a reference to the master oscillator which runs at 1/12 of the required local oscillator frequency.

The ARC-34 tuning system has a three-stages.

The first stage contains three Ledex stepper motors and a relay, coupled with the four digits in the control panel. The stepper motors select the crystals of four oscillators in the crystal reference system (CRS) . Their frequencies are added up to a frequency between 17 and 32 MHz with many mixer products, but with a very precise and stable frequency, called the crystal reference.

The second stage is basically a dc motor, driving many ganged variable capacitors, and a 9 position switch, which divides the total frequency span of 220 – 400 MHz into nine sectors of 20 MHz each. The motor rotates the variable capacitors over 180 degrees in 1.8 seconds, autoreverses, and rotates the same 180 degrees back etcetera. One of these variable capacitors tunes the master oscillator between 17 and 32 MHz. This oscillator is phase-locked to the crystal reference.

The third stage is a reactance tube which fine-tunes the master oscillator.

The difference between master oscillator and the crystal reference is measured and called dFerr.
A special circuit is used to stop the movement of the variable capacitors *on the fly* at the very moment that the error passes zero. The master oscillator is finally phase-locked to the crystal reference with a reactance tube.

When third and fourth digit run from 0.0 to 9.9, the sum of the corresponding crystal frequencies run from 12.0146 to 12.8396 MHz. Together with the 4 … 23d harmonic of the 833.333 kHz oscillator, this gives the crystal reference frequency range of 17-32 MHz.

In the RF module, this frequency is multiplied by 12, and used as local oscillator for the receiver. After adding 15.825 MHz, ( the receiver IF frequency ), it is the transmit frequency.

The lowest xmit frequency is ( 12.0146 + 4 x 0.83333 ) x 12 + 15.825 = 200.0 MHz
The highest xmit frequency is ( 12.8396 + 23 x 0.83333 ) x 12 + 15.825 = 399.9 MHz

# 1. Crystal Reference System

### *1.1 Ledex stepper motors*

The second, third and fourth digit set the position of a low impedance voltage divider in 2.3V steps. The Ledex stepper motors in the RT-236 have similar voltage dividers, and a sensitive relay compares the two divider output voltages, and operate the corresponding stepper motor until the difference is less than 1.6V. The relay is on with 1.6V coil voltage or more, yet is not damaged with 27V. The coil resistance is 230 Ω.
The digit-4 drive relay also interrupts the crystal reference system, to force a small backward step of the tuning motor., otherwise there would be no tuning in case of a 0.1MHz step on the control panel.
The sequence of the Ledex motors is 0-1-2-3-4-5-8-9-8-7-6-3. This means if you change a digit from 1 to 2, there is a single click. If you change from 7 to 8, you hear 11 clicks.

### *1.2 Crystal oscillators.*

The CRS has 4 oscillators, controlled by the four digits of the frequency setting on the control panel. All four oscillators are based on crystals, operated in ovens at 85 deg C.
The first minute after turn-on, the combined ovens take 8A, half of the complete ARC-34 !

The first digit is either 2 or 3, and controls a relay.
The **first and second digit** select a harmonic of a 833.333 kHz oscillator (osc.1)
The second digit selects the 4$^{th}$ to 13$^{th}$ harmonic when set from 0 to 9
The first digit adds 10 times 0.83333 = 8.33333 MHz to this when the first digit is " 3"
The **third digit** selects the crystal frequencies of osc. 2, at 0/1/2/3/4 and again at 5/6/7/8/9
3.233333 / 3.400000 / 3.566667 / 3.733333 / 3.900000 MHz in 1/6 MHz steps;
The **third and fourth digit** select together the four frequencies of osc.3:
Third digit < 5 and fourth digit <5 then osc.3 = 3.650000 MC
Third digit < 5 and fourth digit >4 then osc.3 = 3.691666
Third digit > 4 and fourth digit <5 then osc.3 = 3.733333
Third digit > 4 and fourth digit >4 then osc.3 = 3.775000 in 1/24 MHz Steps;
The **fourth digit** selects the crystal frequencies of osc.4 , at 0/1/2/3/4 and again at 5/6/7/8/9
5.131250 MC5.139583 / 5.147917 / 5.156250 / 5.164583 MHz in 1/120 MHz steps.

When third and fourth digit run from 0.0 to 9.9, the sum of the corresponding crystal frequencies runs from 12.0146 to 12.8396 MHz. Together with the 6 … 23d harmonic of the 833.333 kHz oscillator, this gives a crystal reference frequency in the range of 17-32 MHz.

In the RF module, there is a master oscillator with the same frequency range, this frequency is multiplied by 12, and used as local oscillator for the receiver. After adding 15.825 MHz ( the first IF frequency) , it is the transmit frequency.

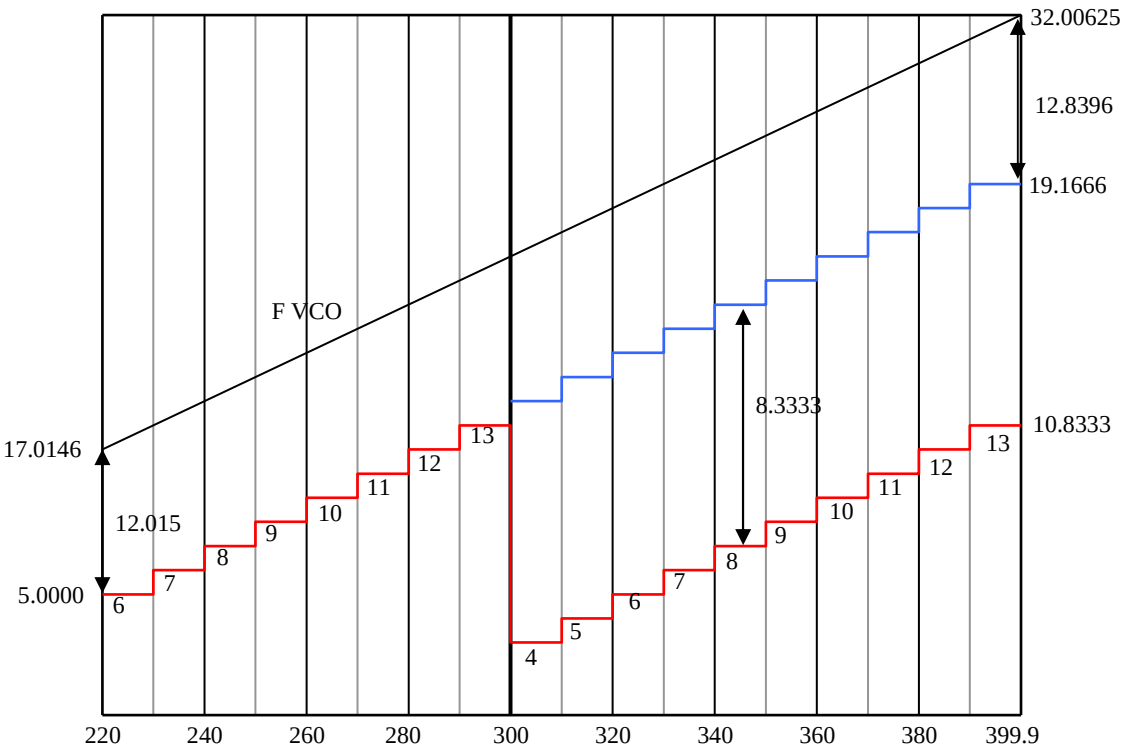
The lowest xmit frequency is ( 12.0146 + 6 x 0.83333 ) x 12 + 15.825 = 220.0 MHz
The highest xmit frequency is ( 12.8396 + 23 x 0.83333 ) x 12 + 15.825 = 399.9 MHz

**Exceptions**
The crystal reference system can handle any number as 2$^{nd}$, 3d or 4$^{th}$ digit, so the range would be 200-399.9 MHz.
However, the variable capacitors tuning system has a smaller range, 220 – 399.9 MHz, divided into 9 sectors of 20 MHz each. The master oscillator tunes from approx. 223 - 403 MHz.
The phase locked loop is disabled during:
- Stepping of the digit-4 ledex motor, and
- during the reverse part of the motor cycle.

### *1.3 Mixers*

The first mixer compares the VCO frequency with the oscillator 1 frequency ( plus 8.333 MHz when the first digit is “3”)
This gives a first intermediate frequency of 12.01 – 12.84 MHz.
The second mixer compares this with the oscillator 2 frequency.
This gives a second intermediate frequency of 8.78 - 8.94 MHz
The third mixer compares this with the oscillator 3 frequency
This gives a third intermediate frequency of 5.13 - 5.16 MHz
Finally, this signal is compared with the signal from oscillator 4 in a phase detector, and should result in zero Hz when locked. This is the dF err signal.
With 1 kHz difference, the output of the phase comparator is a 1 kHz sinewave of approx. 30 Vpp
With more than 5 kHz difference, dFerr is zero. The channel distance is 100kHz/12 = 8 kHz

The frequency of the VCO (black) , and that of osc.1 (red) are shown in this plot, with the control panel dial setting on the X-axis.




**Adjustments.**
The intermediate frequency filters are factory tuned inside a hermetic seal.
The first oscillator has 3 trim caps ( 2 for frequency, one for amplitude)
The third mixer has a bias level pot. No idea how to adjust these.

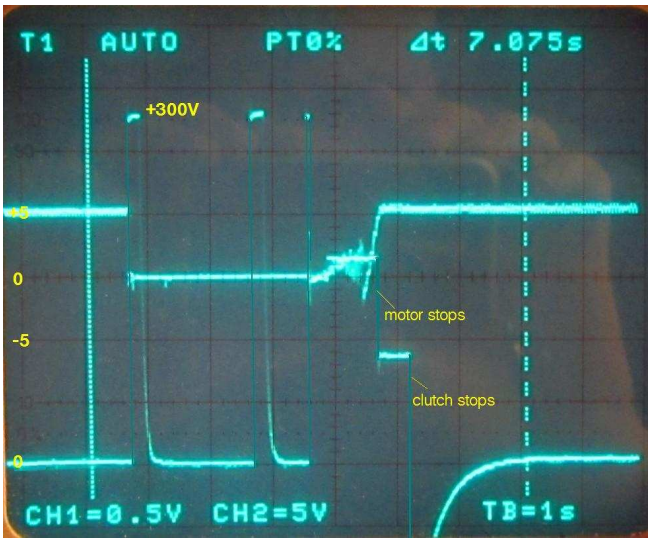
**Use of dFerr**
The output of the Crystal Reference System , the dF error, is fed both to
1) the motor controller , which does the coarse tuning of the master oscillator and all doubler and tripler circuits,
2) and to a reactance tube, which phase-locks the master oscillator to the CRS.

### *1.4 Mechanical system*

The mechanical system consists of a motor, dual ratio gearbox and a brake.
The motor is electrically reversed when reaching each of the endstops, but only the upward cycle is used for phase locking.
All variable capacitors are coupled, and driven from a dc motor either in high gear, corresponding with 100 MHz/sec ( 1.8 sec from min to max or v.v.), or with low gear at approx – 3MHz/sec.
Tuning is done at high gear until the desired frequency is passed, followed by a low gear movement in opposite direction to allow the PLL system to lock.
The coil operated brake on the motor is released when the motor is powered. When the PLL locks, the motor is switched off, and the brake stops the motor quickly.

### *1.5 Lock cycle*

The circuit is shown below. Normally, dFerr is +5V, the tuning is in the right sector, K1 is ON, and the motor is OFF. ( Relay K1 turns off the motor)

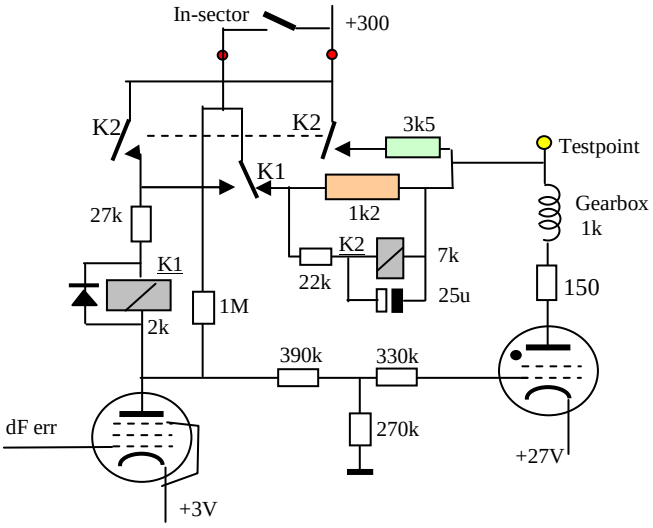


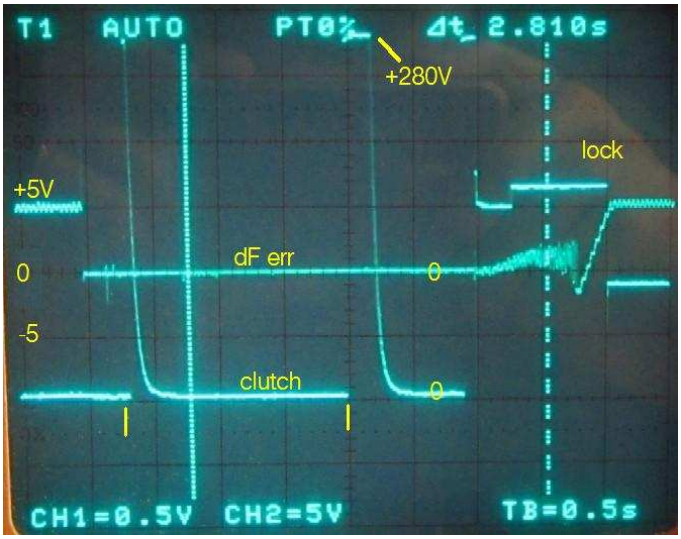

In this picture, the upper trace is the voltage on the top of the gearbox coil, the lower trace is the dF error.
Time is 1 sec/div. The whole tuning process takes less than 4 seconds.

The capacitor shaft rotates two half cycles, passing each time the correct sector, as indicated by 300V pulses on the top of the gearbox coil.
Halfway the third passage of the correct sector, dFerr makes a sharp negative pulse, which turns on the thyratron and the gearbox coil, so the frequency now walks back slowly. The current in the gearbox coil turns on K2 after 0.2 sec. When the PLL locks, dFerr goes positive, turning-on K1 which stops the motor. Finally K2 and the gearbox are turned off.

In short the 3 actions:

1) Rotate until the correct sector is reached and a sharp negative peak in dF-err occurs. This gives a positive pulse to the thyratron, and the gearbox coil is energized (thyratron stays ON)
With current in the gearbox coil, relay K2 will turn ON with 0.3 sec delay.
With the gearbox powered, the variable capacitors move backwards at low speed
2) Once K2 is ON, relay K1 will turn ON when dFerr goes positive, and stays on. The motor stops.
3) After some delay, K2 drops OFF, and the gearbox is reset to high gear.



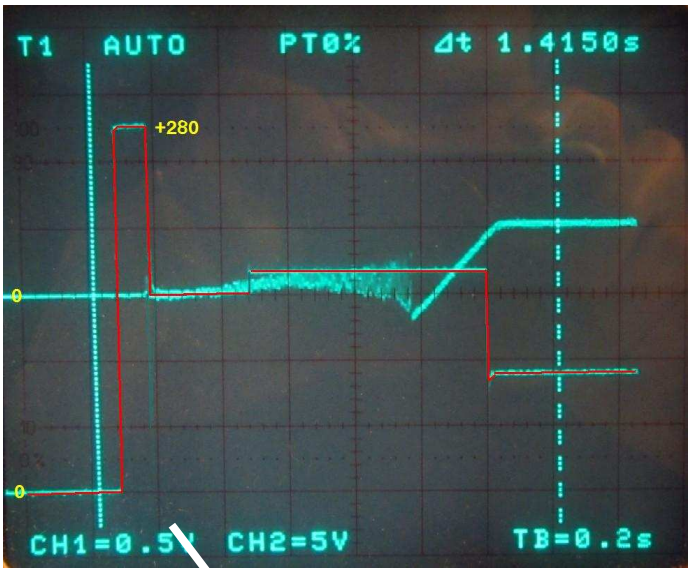



Tuning process

dFerr 5V/div ( via x10 probe)
Gearbox voltage 50V/div ( via x10 probe)

Time 0.5 sec /div

Freq change upward(?) with two full half-cycles of the variable capacitors.

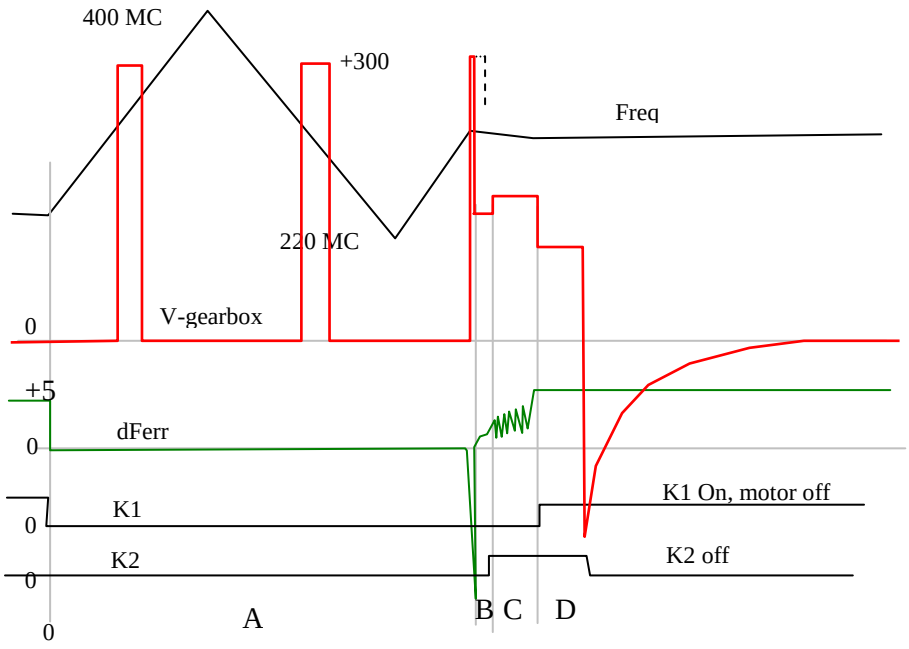


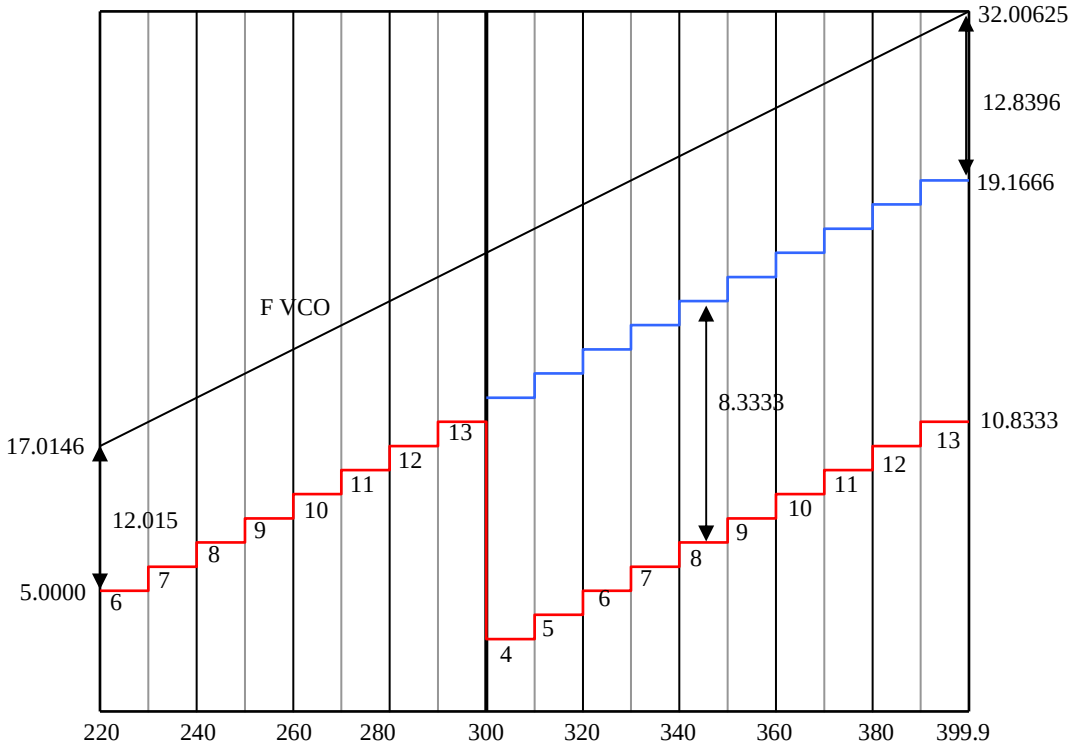

Freq change downward

Time 0.2 sec/div. At this sweepspeed, the glitch in dFerr is just visible.

The beat frequency between crystal reference and master oscillator is visible in the dFerr signal, and used to phase-lock the master oscillator to the crystal reference.
When the phase lock is complete, the dF err signal goes positive, and K1 turns on, stopping the motor completely.


Detail
Same recording, expanded to 20ms/div.
Ths glitch in dFerr is clearly visible and lasts only 3ms until the thyratrons fire.
This turns-on the gearbox, and initiates the phase-lock procedure.


400 MC
+300
Freq
220 MC
V-gearbox
0
+5
dFerr
0
K1
0
K1 On, motor off
K2
0
K2 off
0
A
B C D


32.00625
12.8396
19.1666
F VCO
8.3333
10.8333
17.0146
12.015
5.0000
4
5
6
7
8
9
10
11
12
13
220
240
260
280
300
320
340
360
380
399.9